

In re Patent Application of:
CORONEL ET AL.
Serial No. 10/042,520
Filing Date: January 9, 2002

In the Specification:

Please replace the paragraph beginning at page 6, line 32, with the following rewritten paragraph:

Figure 2 is a diagram illustrating the steps to be implemented to insert the bit line contact in the architecture according to the prior art; and

Please replace the paragraph beginning at page 6, line 35, with the following rewritten paragraph:

Figures 3 to 9 are diagrams illustrating the different steps of the method according to the invention.
invention; and

Please insert the following paragraph on page 7, line 2:

Figure 10 is a block diagram of an integrated circuit with an embedded DRAM according to the invention.

Please replace the paragraph beginning at page 10, line 1, with the following rewritten paragraph:

According to a specific embodiment of the invention, the polysilicon layer poly3 implantation step is preceded by an additional step. This step is necessary when the method according to the invention is applied to the production of an embedded DRAM memory. The purpose of this step is to prevent

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the implantation of the polysilicon layer poly3 located in the logic zones of the chip. An integrated circuit 20 including an embedded DRAM 22 is illustrated in Figure 10, for example.

Bus 24 connects the embedded DRAM 22 to the logic circuitry

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